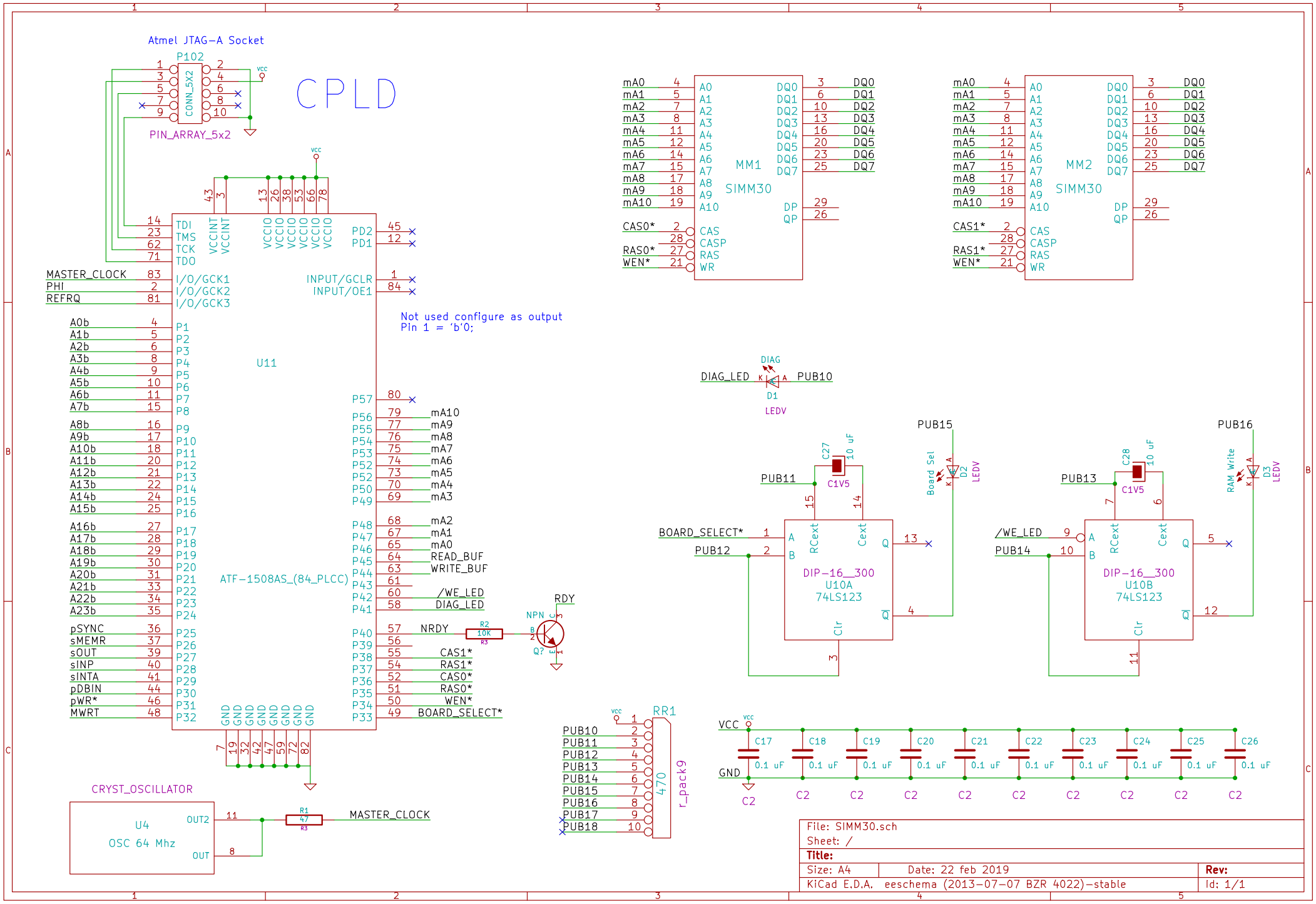

Atmel JTAG-A Socket
P102
CONN_5X2
PIN_ARRAY_5x2
CPLD
U11
ATF-1508AS_(84_PLCC)
Not used configure as output
Pin 1 = 'b'0;
MASTER_CLOCK
PHI
REFRQ
A0b
A1b
A2b
A3b
A4b
A5b
A6b
A7b
A8b
A9b
A10b
A11b
A12b
A13b
A14b
A15b
A16b
A17b
A18b
A19b
A20b
A21b
A22b
A23b
pSYNC
sMEMR
sOUT
sINP
sINTA
pDBIN
pWR*
MWRT
mA10
mA9
mA8
mA7
mA6
mA5
mA4
mA3
mA2
mA1
mA0
READ_BUF
WRITE_BUF
/WE_LED
DIAG_LED
NRDY
CAS1*
RAS1*
CAS0*
RAS0*
WEN*
BOARD_SELECT*
RDY
NPN
Q?
R2
10K
R3
MM1
SIMM30
MM2
SIMM30
CAS0*
RAS0*
WEN*
CAS1*
RAS1*
DIAG
D1
LEDV
PUB10
PUB11
PUB12
PUB13
PUB14
PUB15
PUB16
C27
10 uF
C1V5
C28
10 uF
C1V5
Board Sel
D2
LEDV
RAM Write
D3
LEDV
DIP-16__300
U10A
74LS123
DIP-16__300
U10B
74LS123
RCext
Cext
Clr
RR1
470
r_pack9
VCC
GND
C17
C18
C19
C20
C21
C22
C23
C24
C25
C26
0.1 uF
C2
CRYST_OSCILLATOR
U4
OSC 64 Mhz
OUT2
OUT
R1
47
R3
MASTER_CLOCK
File: SIMM30.sch
Sheet: /
Title:
Size: A4
Date: 22 feb 2019
Rev:
KiCad E.D.A. eeschema (2013-07-07 BZR 4022)-stable
Id: 1/1